

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claims 1-4 (canceled)

1 **Claim 5 (currently amended):** A semiconductor device,
2 which is formed by combining and disposing pre-registered
3 functional blocks, and determining a wiring pattern in
4 accordance with a given logic circuit specification,
5 wherein:

6 ~~each of~~ at least one of the functional blocks has a
7 logic circuit and a diode; and

8 the diode is composed of a first conduction type
9 diffusion layer and a second conduction type well connected
10 to a power source, ~~the diode being connected to an input~~
11 ~~terminal, which is to be potential-clamped, among input~~
12 ~~terminals of the functional blocks~~

13 the diode is connected to a potential-clamped input
14 terminal of the at least one of the functional blocks.

1 **Claim 6 (previously presented):** The semiconductor
2 device as claimed in Claim 5, wherein the logic circuit is
3 a memory.

1 **Claim 7 (currently amended):** A method of designing a
2 semiconductor device, which is formed by combining and
3 disposing pre-registered functional blocks, and determining
4 a wiring pattern in accordance with a given logic circuit
5 specification, comprising the steps of:

6 registering the functional blocks in advance,
7 wherein ~~each of~~ at least one of the functional blocks
8 has a logic circuit and a diode, and

9 wherein the diode is composed of a first conduction
10 type diffusion layer and a second conduction type well
11 connected to a power source, ~~the diode being connected to~~
12 ~~an input terminal, which is to be potential-clamped, among~~
13 ~~input terminals of the functional blocks~~

14 the diode is connected to a potential-clamped input
15 terminal of the at least one the functional blocks.

1 **Claim 8 (previously presented):** A computer-readable
2 recording medium, on which the method of designing a
3 semiconductor device, as claimed in Claim 7, is stored as
4 a program to be executed by a computer.

1 **Claim 9 (currently amended):** A design support
2 apparatus for a semiconductor device, which is formed by
3 combining and disposing pre-registered functional blocks,
4 and determining a wiring pattern in accordance with a given
5 logic circuit specification, comprising:

6 registration means for registering the functional
7 blocks in advance,

8 wherein ~~each of~~ at least one of the functional blocks
9 has a logic circuit and a diode, and

10 wherein the diode is composed of a first conduction
11 type diffusion layer and a second conduction type well
12 connected to a ~~power source, the diode being connected to~~
13 ~~an input terminal, which is to be potential-clamped, among~~
14 input terminal[[s]] of the at least one of the functional
15 blocks.

1 **Claim 10 (new):** A semiconductor device which is formed
2 by combing and disposing pre-registered functional blocks,
3 and determining a wiring pattern in accordance with a given
4 logic circuit specification, wherein:

5 at least one of the functional blocks including
6 functional blocks has a logic circuit and a diode which is
7 at least connected to an input pin where results of an
8 antenna ratio exceed an allowed antenna ratio; and

9 the diode is composed of a first conduction type
10 diffusion layer and a second conduction type well connected
11 to a power source,

12 the diode is connected a potential-clamped input
13 terminal of the at least one of the functional blocks.

1 **Claim 11 (new):** The semiconductor device as claimed in

2 Claim 10, wherein the logic circuit is a memory.

1 **Claim 12 (new):** A method of designing a semiconductor
2 device, which is formed by combining and disposing pre-
3 registered functional blocks, and determining a wiring
4 pattern in accordance with a given logic circuit
5 specification, comprising the steps of:

6 registering the functional blocks in advance,

7 wherein at least one of functional blocks has a logic
8 circuit and a diode which is at least connected to an input
9 pin where results of an antenna ratio exceed an allowed
10 antenna ration;

11 wherein the diode is composed of a first conduction
12 type diffusion later and a second conduction type well
13 connected to a power source,

14 the diode is connected to a potential-clamped input
15 terminal of the at least one of the functional blocks.

1 **Claim 13 (new):** A computer-readable recording medium,
2 on which the method of designing a semiconductor device, as
3 claimed in Claim 12, is stored as a program to be executed
4 by a computer.

1 **Claim 14 (new):** A design support apparatus for a
2 semiconductor device, which is formed by combining and
3 disposing pre-registered functional blocks, and determining

4 a wiring pattern in accordance with a given logic circuit
5 specification, comprising:

6 registration means for registering the functional
7 blocks in advance,

8 wherein at least one of the functional blocks has a
9 logic circuit and a diode which is at least connected to an
10 input pin where results of an antenna ratio exceed an
11 allowed antenna ratio, and

12 wherein the diode is composed of a first conduction
13 type diffusion layer and a second conduction type well
14 connected to a potential-clamped input terminal of the at
15 least one of the functional blocks.